Part I

Cascode Amplifier Specifications:

(1) $\mathrm{R_{out}}$ maximum at mid band $= 5\mathrm{k\Omega}$

(2) $\mathrm{R_{in}}$ range at mid band $= 2.5 - 10\mathrm{k\Omega}$

(3) $|\mathrm{A_v}|$ minimum value at mid band $= 50$

(4) $\mathrm{f_l}$ maximum value at low f cut in $= 500\mathrm{Hz}$

Biasing the Cascode:

To bias the cascode and find all the component values I will use the ¼ rule. I know that

Vcc = 20V, CB = 500uF, from Mini Project II I know that β for the 2N2222A transistor = 170.

$$V_{C2} = \frac{3}{4}V_{CC} = 15V$$

$$V_{C1} = \frac{1}{2}V_{CC} = 10V$$

$$V_{E2} = \frac{1}{2}V_{CC} = 10V$$

$$V_{E1} = \frac{1}{4}V_{CC} = 5V$$

$$V_{B2} = V_{E2} + V_{BE} = 10.7V$$

$$V_{B1} = V_{E1} + V_{BE} = 5.7V$$

R_{out} is constrained to be a maximum of 5kΩ and $R_{out} = R_C$, so picking from the standard resistors list I can simply set R_C to be 4.7kΩ.

$$I_{C2} = \frac{20 - 15}{4.7k} = 1.06mA$$

$$I_{B2} = \frac{I_{C2}}{\beta} = 6.26uA$$

$$I_{C1} = I_{C2} + I_{B2} = 1.07mA$$

$$I_{B1} = \frac{I_{C1}}{\beta} = 6.29uA$$

$$I_{E2} = I_{C2} + I_{B2} = 1.07mA$$

$$I_{E1} = I_{B1} + I_{C1} = 1.08mA$$

$$I_1 = 0.1I_{E1} = 107.64uA$$

$$I_2 = I_1 - I_{B2} = 101.38uA$$

$$I_3 = I_2 - I_{B1} = 95.09uA$$

$$R_{B1} = \frac{V_{CC} - V_{B2}}{I_1} = 86.4k\Omega$$

$$R_{B2} = \frac{V_{B2} - V_{B1}}{I_2} = 49.3k\Omega$$

$$R_{B3} = \frac{V_{B1}}{I_3} = 59.9k\Omega$$

$$R_E = \frac{V_{E1}}{I_{E1}} = 4.6k\Omega$$

By choosing the closest values from the standard values list

$$R_{B1} = 82k\Omega$$

$$R_{B2} = 51k\Omega$$

$$R_{B3} = 62k\Omega$$

$$R_E = 4.7k\Omega$$

Calculating the small signal parameters:

$$\beta = 170$$

$$g_{m2} = \frac{I_{C2}}{V_T} = 0.042\mho$$

$$r_{\pi 2} = \frac{\beta}{g_m} = 4k\Omega$$

$$g_{m1} = \frac{I_{C1}}{V_T} = 0.043\mho$$

$$r_{\pi 1} = \frac{\beta}{g_m} = 3.97k\Omega$$

Calculating the capacitances C_{C1},C_{C2}, and C_E:

C_{C1},C_E can be calculated by the method of short and open circuit time constants

$$\tau_{CC1}^{OC} = C_{C1}[R_S + R_{B2}||R_{B3}||(r_{\pi 1} + (1 + \beta)R_E)]$$

$$= C_{C1}[27.09k\Omega]$$

$$\tau_{CE}^{SC} = C_E[\frac{r_{\pi 1} + R_S||R_{B2}||R_{B3}}{1 + \beta}||R_E]$$

$$= C_E[23.4\Omega]$$

$$\omega_{L3dB} = 500Hz \times \frac{2\pi}{Hz} = \sqrt{\left(\frac{1}{23.4C_E}\right)^2 - 2\left(\frac{1}{R_E C_E}\right)^2}$$

$$C_E = 13.6uF$$

The coupling capacitors can be set to the same value

$$C_{C1} = 13.6uF$$

$$C_{C2} = 13.6uF$$

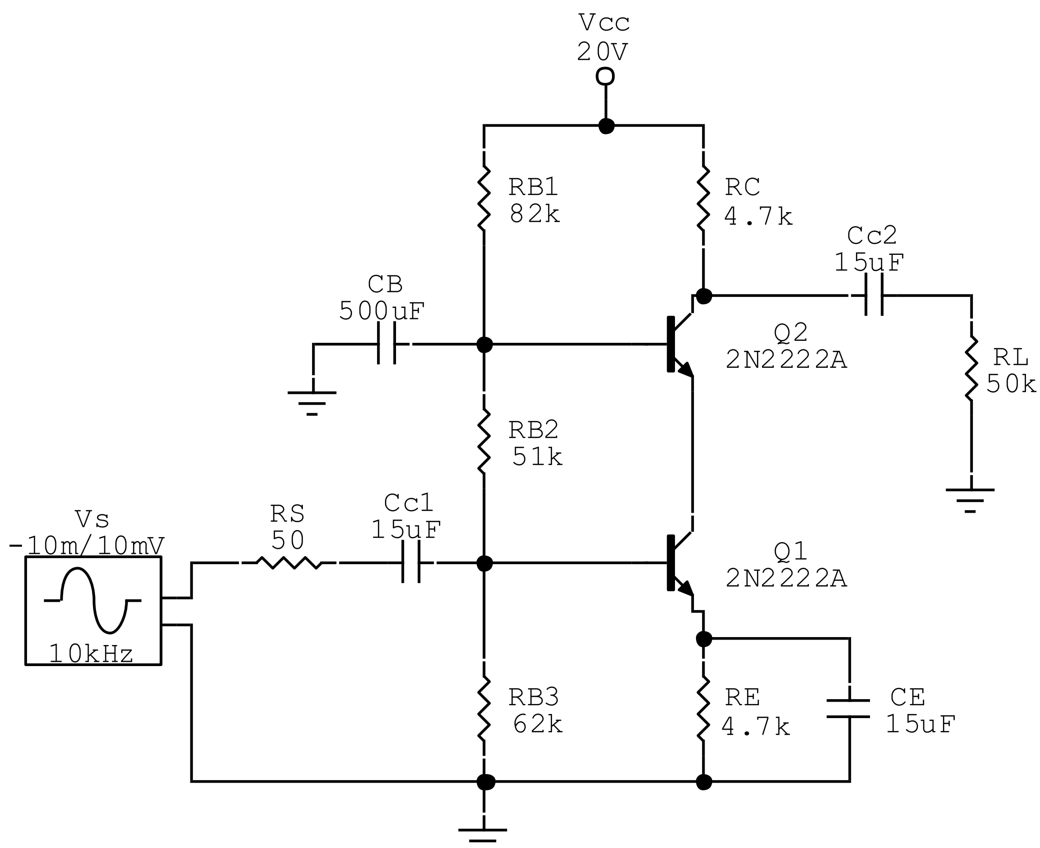
By choosing a value from a standard list of capacitors close to this number and making sure also to satisfy $f_l\ maximum\ value\ at\ low\ f\ cut\ in = 500Hz$ as per requirement (4)

$$C_E = 15uF$$

$$C_{C1} = 15uF$$

$$C_{C2} = 15uF$$

A.



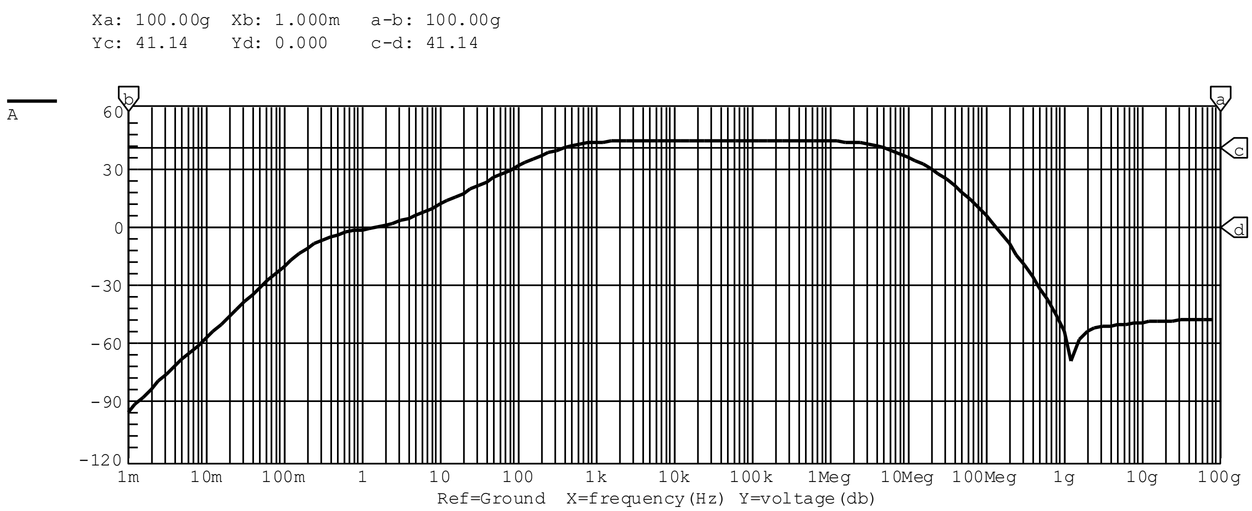
Complete Cascode Circuit

D.C. Operating Point

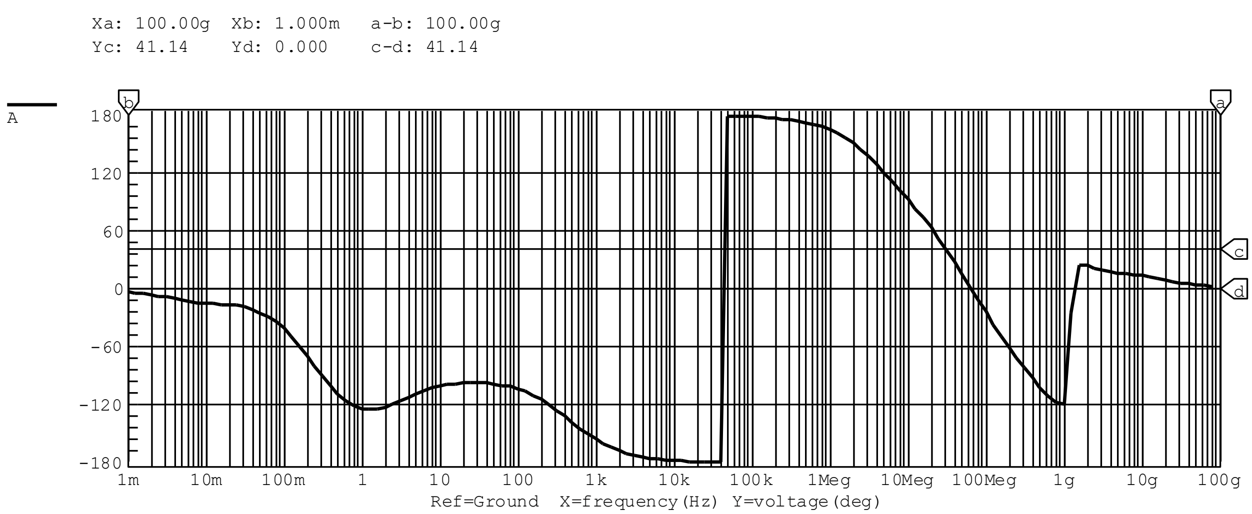
	V_B	V_C	V_E	I_B	I_C	I_E
Q_1	5.905V	10.50V	5.301V	6.643uA	1.123mA	1.129mA
Q_2	11.10V	14.76V	10.50V	6.657uA	1.116mA	1.123mA

B.

These plots can be used to approximate ω_{L3dB} and ω_{H3dB}



Magnitude Plot



Phase Plot

Calculation of the low and high 3dB points:

For the low frequency response, we can calculate ω_{L3dB} as follows

$$\omega_{L3dB} = \frac{1}{C_E[\frac{r_{\pi 1} + R_S||R_{B2}||R_{B3}}{1+\beta}||R_E]}$$

$$\omega_{L3dB} = \frac{1}{15uF \times 23.4\Omega}$$

$$\omega_{L3dB} = 2.85krad/s$$

For the high frequency response, we can calculate ω_{H3dB} as follows

$$\omega_{H3dB} = \frac{1}{c_u \times (R_L||R_C)}$$

$$\omega_{H3dB} = \frac{1}{8pF \times (50k||4.7k)}$$

$$\omega_{H3dB} = 29.1Mrad/s$$

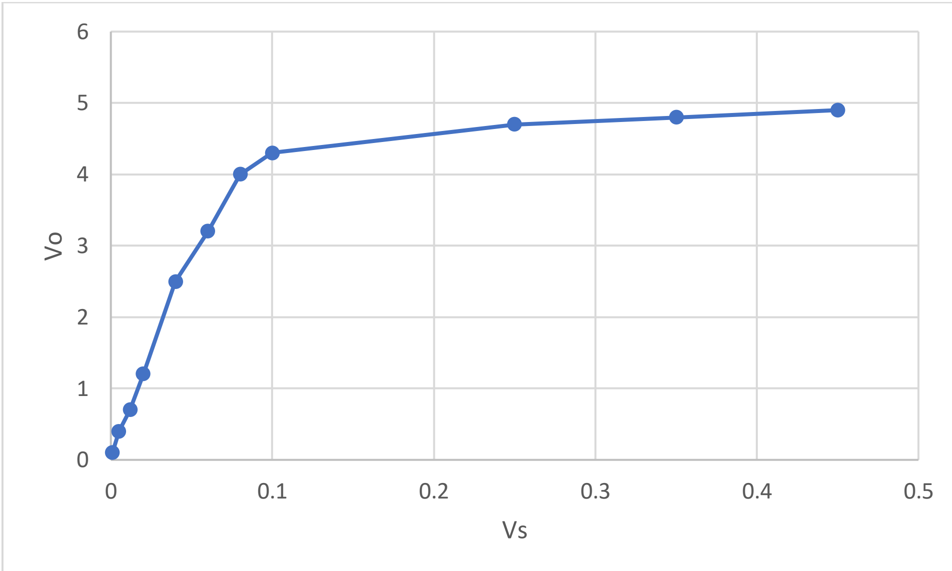
Comparison of measured and calculated 3dB points:

	Measured	**Calculated**
$\boldsymbol{\omega_{L3dB}}$	$2.96krad/s$	$2.85krad/s$
$\boldsymbol{\omega_{H3dB}}$	$54.8Mrad/s$	$29.1Mrad/s$

Discussion[Calculated vs Measured Values]:

- The locations of the high and low 3dB points can be approximated quite accurately using the dominant pole for each respective 3dB point. The measured locations of the poles, however, bear some inaccuracy when compared to the calculated values. It should be noted that the low 3dB point values are very close to one another (within 5%), whereas the high 3dB measured value is significantly different from the calculated one. This is due to the miller transformation that is needed to deal with the high frequency capacitor c_u which introduces some differences in the calculated results.

C.



Discussion[Vo/Vs Plot]:

- At this mid band frequency, it is clear where the Vo/Vs relationship stops being linear. This occurs when the transistor is saturated and outside of the active region where it should be operating. In this linear region it can be seen that $|\mathrm{A_v}| > 50$ as per requirement (3) of the cascode amplifier specifications.

D.

Calculated input impedance:

The input impedance is given by

$$R_{in} = r_{\pi 1}||R_{B2}||R_{B3}$$
$$= 3.48k\Omega$$

Measured input impedance:

R_{in} can be measured by applying a test source to the input node. I will disregard the effect of the source impedance R_S

$$R_{in} = \frac{V_{TEST}}{I_{TEST}}$$

$$= \frac{8.42mV}{2.24uA}$$

$$= 3.76k\Omega$$

Discussion[Measured vs Calculated Impedance]:

- The calculated and measured input impedances match each other quite nicely which is reassuring that the methods used are adequate. More importantly, both values fall within the range of values given in requirement (2) of the cascode amplifier specifications.

Summary[Part I]:

- In this section, the cascode amplifier was examined. The ¼ rule was implemented to bias the transistor and obtain values for the various resistance values. Then, by using a standard list of values, resistors that would be available in industry were placed into the circuit. Building off previous mini projects, the method of short and open circuit time constants was used in order to find values for both coupling capacitors and also C_E. From the bode plots, the low and high 3dB points were calculated. These points were then compared with the values calculated by hand and insights regarding the similarities and differences were explored. The voltage relationship between the input and output was examined at mid band. In the linear region it was confirmed that the gain did indeed stay above 50$\frac{v}{v}$ as per the requirements. Finally, the input impedance was calculated and compared with the one measured by using a test source at the input node. Both these values fell within the acceptable range, once again providing confidence in the methods and tools used.

Part II

A.

Biasing the cascade:

It is stated in the requirements for R_{in} and R_{out} to be $50\Omega \pm 5\Omega$

$$R_{in} = R_E || \frac{r_{\pi 1}}{1+\beta_1}$$

$$\approx \frac{V_T}{I_{E1}}$$

Then, if we know V_T = 25mV and R_{in} = 50Ω, it follows that

$$I_{E1} = 0.5mA$$

Knowing this, I will begin to bias the circuit using $V_{E1} = \frac{1}{3}V_{CC}$ as per the instructions

$$V_{E1} = \frac{1}{3}V_{CC} = 4V$$

$$V_{B1} = V_{E1} + V_{BE} = 4.7V$$

$$V_{B2} = \frac{2}{3}V_{CC} = 8V$$

$$V_{C1} = \frac{2}{3}V_{CC} = 8V$$

$$V_{E2} = V_{B2} - V_{BE} = 7.3V$$

The currents can be calculated because I_{E1} is known and from the previous mini project, β = 165 for the 2N3904

$$I_1 = 0.1 I_{E1} = 50uA$$

$$I_{B1} = \frac{I_{E1}}{1+\beta} = 3.01uA$$

$$I_2 = I_1 - I_{B1} = 47uA$$

$$I_{C1} = \beta I_{B1} = 497uA$$

Next, the resistances can be calculated

$$R_{E1} = \frac{V_{E1}}{I_{E1}} = 8k\Omega$$

$$R_{B1} = \frac{V_{CC} - V_{B1}}{I_1} = 146k\Omega$$

$$R_{B2} = \frac{V_{B1}}{I_2} = 100k\Omega$$

The remaining resistors can be calculated by using the following sets of equations

$$R_{C1} = \frac{V_{CC} - V_{C1}}{I_3}$$

$$R_{out} = \frac{R_{C1} + r_{\pi 2}}{1 + \beta} || R_{E2}$$

$$I_3 = I_{C1} + I_{B2}$$

$$I_{B2} = \frac{I_{E2}}{1 + \beta}$$

$$I_{E2} = \frac{V_{E2}}{R_{E2}}$$

And from the problem requirements R_{out} must be $50\Omega \pm 5\Omega$

$$R_{C1} = 7.6k\Omega$$

$$R_{E2} = 1.6k\Omega$$

The coupling capacitors can be found by utilizing the method of short and open circuit time constants

$$\tau_{CC1}^{SC} = [\frac{r_{\pi 1}}{1 + \beta} || R_{E1}] C_{C1}$$

$$= 50 C_{C1}$$

And due to the fact that C_{C2} sees a similar resistance, we can find $C_{C1,2}$ as follows

$$1000Hz \times \frac{2\pi}{Hz} = \sqrt{\left(\frac{1}{C_{C1}50}\right)^2 + \left(\frac{1}{C_{C2}50}\right)^2}$$

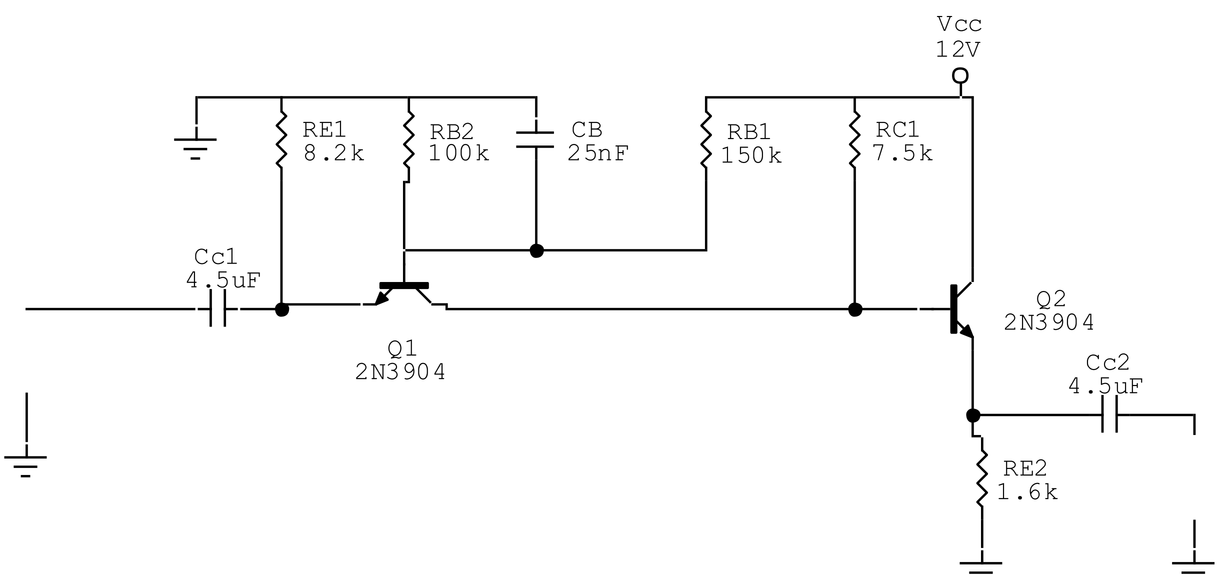
$$C_{C1} = C_{C2} = 4.5uF$$

C_B must be set as small as possible without effecting the low frequency cut in

$$C_B = 25nF$$

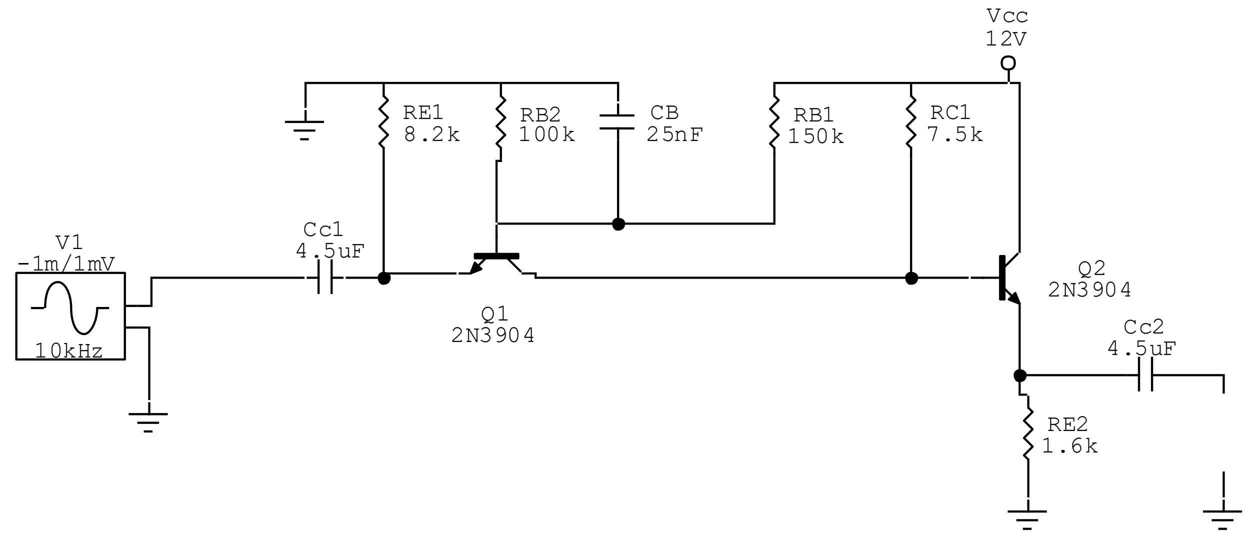
B.

By wiring up the circuit with the closest industry standard values for the resistors and capacitors, I can measure R_{in}, R_{out}, and A_M at mid band



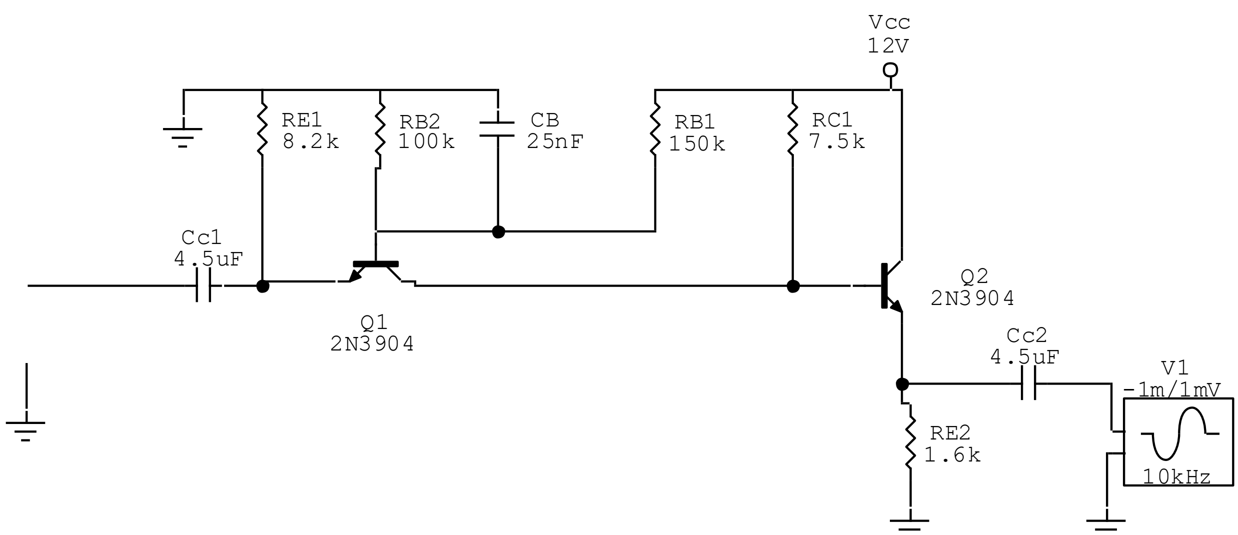
Biased Circuit with Standard values

I can measure R_{in} and R_{out} by applying a Test source to either the input or output node



Circuit to measure R_{in}

$$R_{in} = 51.36\Omega$$



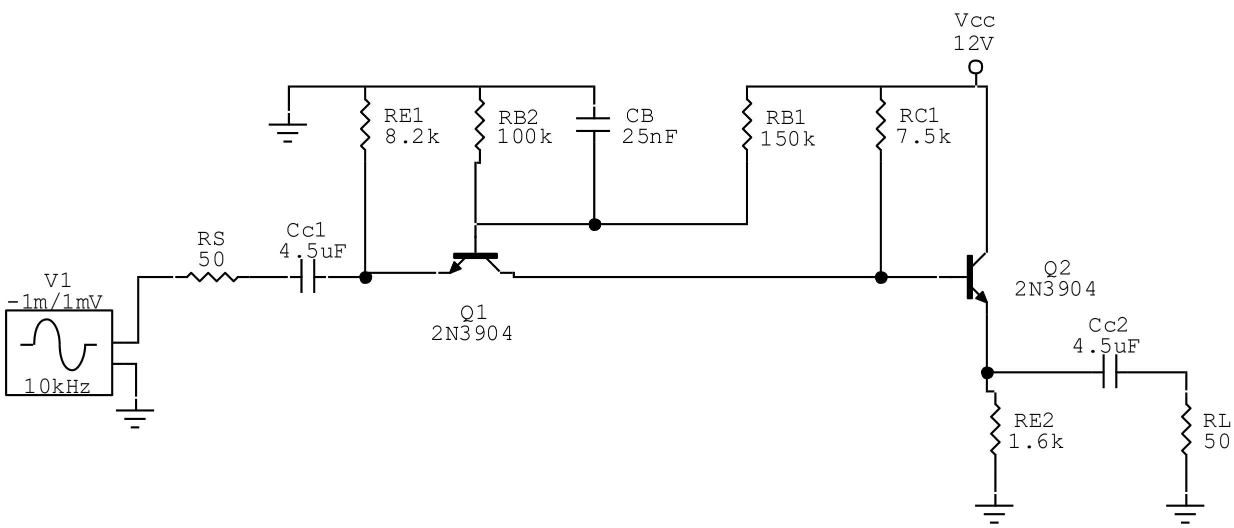
Circuit to measure R_{out}

$$R_{out} = 54.86k\Omega$$

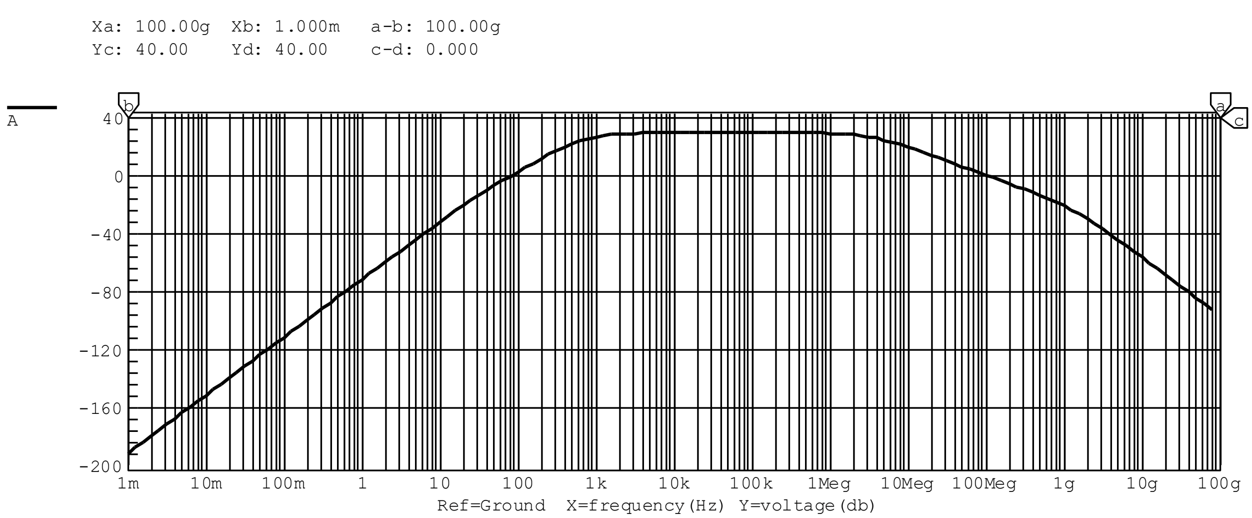
The gain A_M can be found by using the oscilloscope at a mid band frequency. Note, I did not include a source impedance from the generator or a load impedance as per the instructions

$$A_M = 128.57 \frac{V}{V}$$

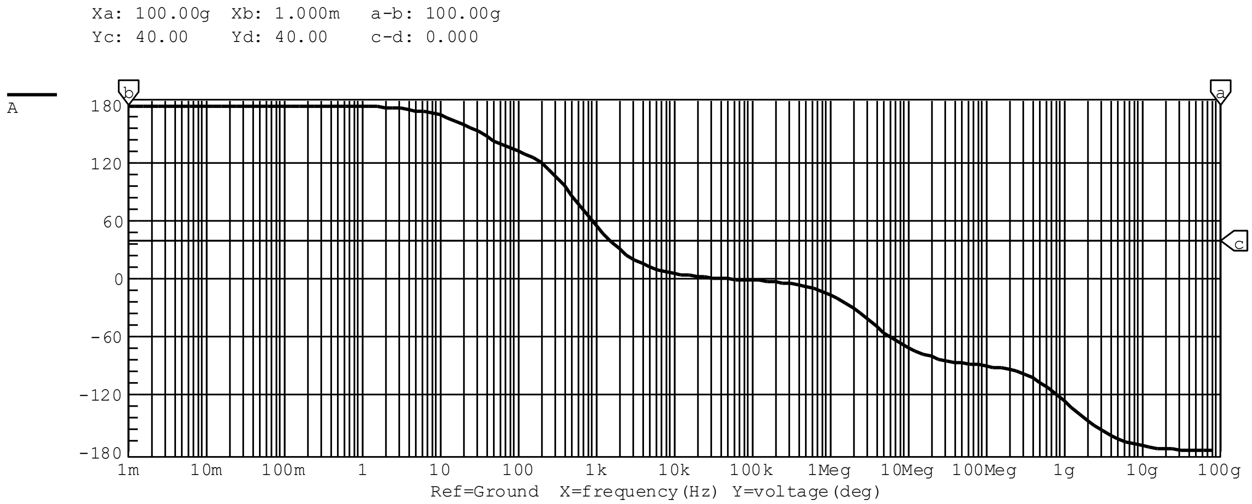
C.



Circuit with source and load impedances attached



Magnitude Plot



Phase Plot

Using this I can find the low frequency cut in and the high frequency cut off

$$Low\ frequency\ cut\ in = 927Hz$$

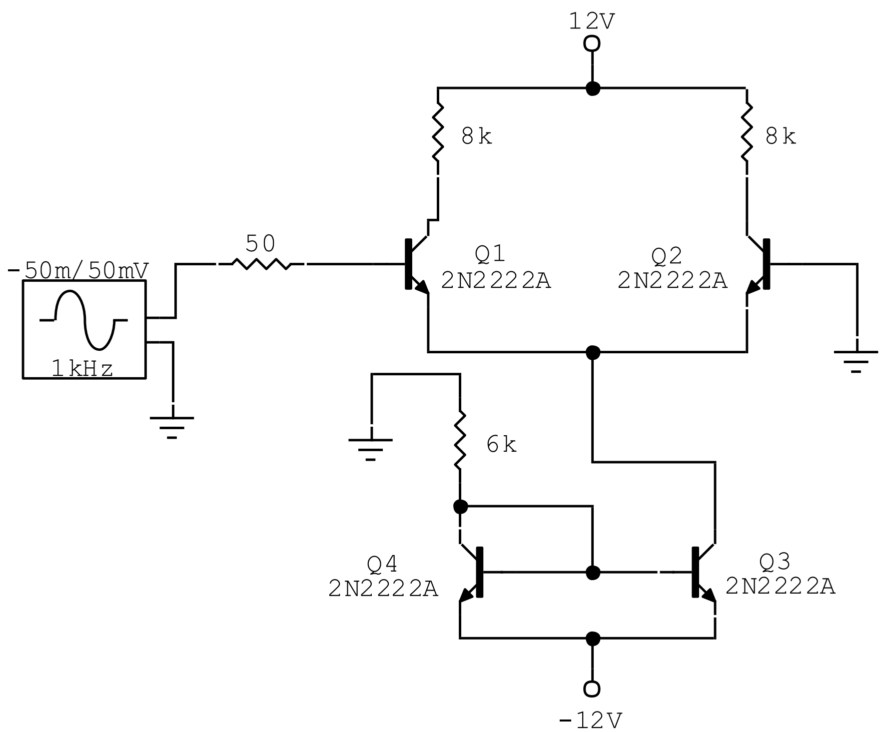
$$High\ frequency\ cut\ out = 3.28MHz$$

Summary[Part II]:

- In this section, the 2N3904 transistor was put in cascade with itself to create a repeater in an analog system. First, the circuit was biased using the 1/3 rule and once the associated resistances and capacitances were found, they were matched with the closest industry standard value. Next, input and output impedances were measured. The instructions specified that these values both be $50\Omega \pm 5\Omega$, and after the measurement it was clear that the values obtained were indeed within this constraint. Finally, bode plots were obtained and the cut in and cut out frequencies were acquired. This section illustrated why putting transistors in cascade is so beneficial and how the methods and tools taught in class to bias circuits can indeed satisfy the given constraints.

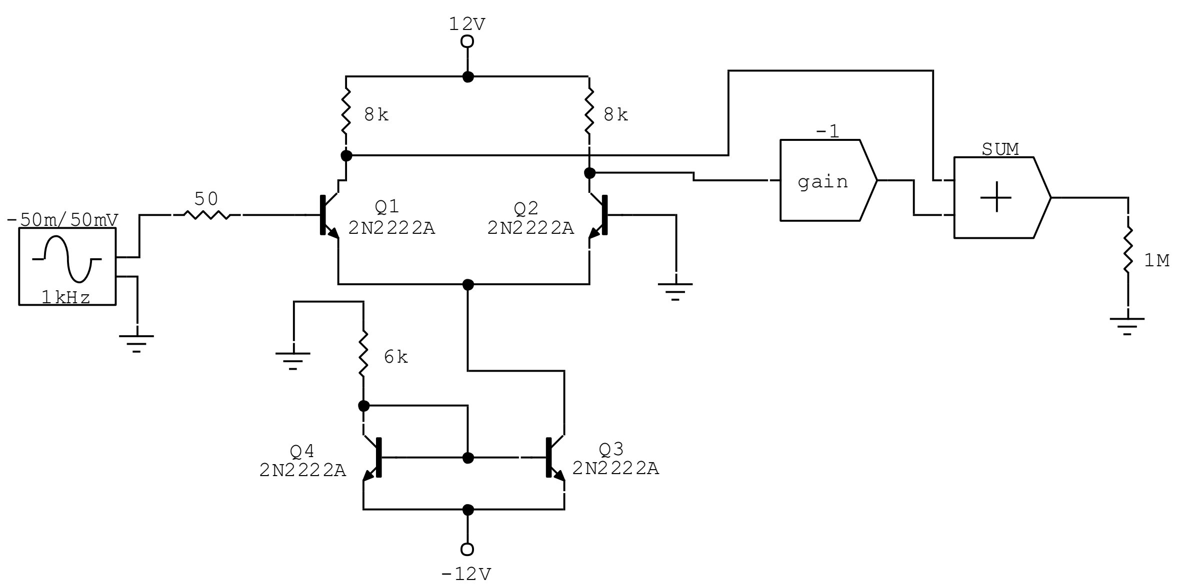
Part III

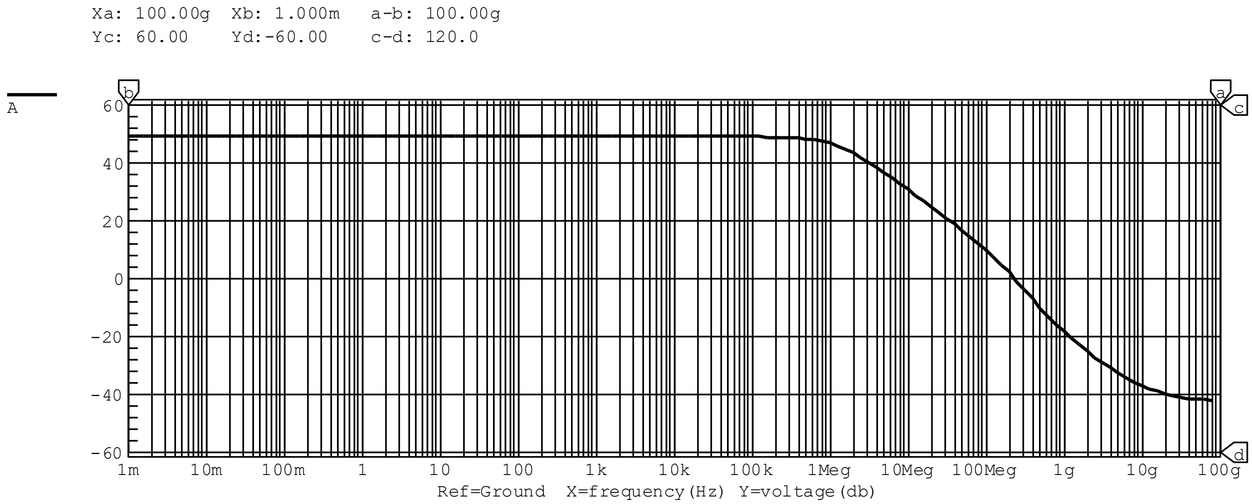
A.



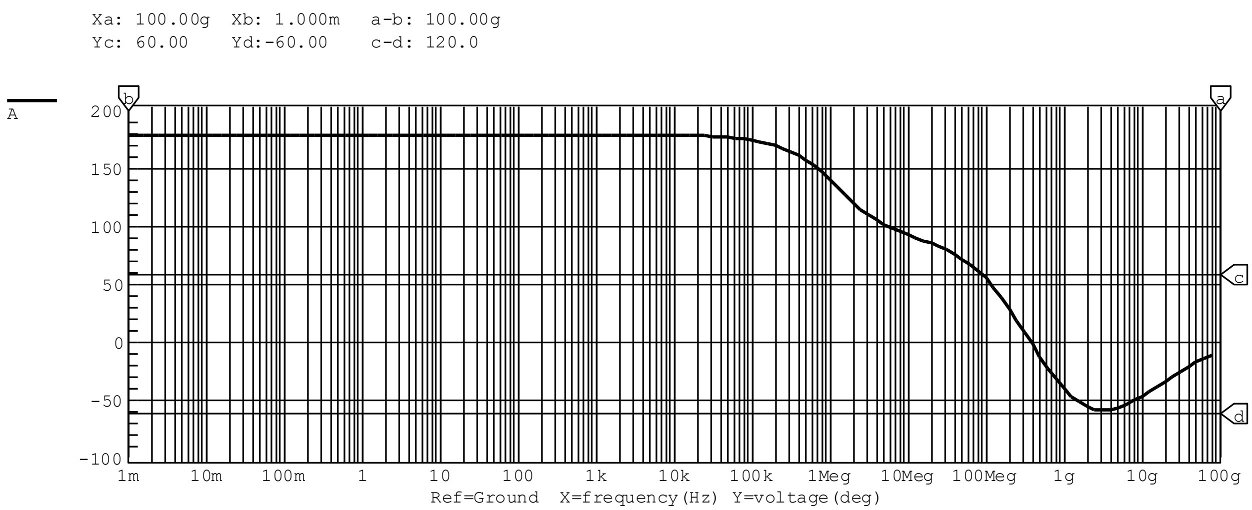
Differential Amplifier Circuit

In order to measure the output Vo across the middle of the circuit I have used a gain block with a gain of -1 and an adder block





Magnitude Plot



Phase Plot

From these plots the high 3dB frequency can be measured to be approximately 7.26MHz

$$f_{H3dB} = 7.26MHz$$

The gain can also be measured by setting the frequency to somewhere in the mid band range and utilizing the oscilloscope

$$A_d = -168\frac{V}{V}$$

B.

Frequency Response of the Differential Amplifier:

The mid band gain can be calculated as follows, I will use a 10MΩ load resistor to ensure it draws virtually no current

$$A_d = \frac{Vo}{Vs} = -g_m R_C \left(\frac{2r_\pi}{2r_\pi + R_S}\right)\left(\frac{R_L}{R_L + 2R_C}\right)$$

$$A_d = -159.2\frac{V}{V}$$

The high 3dB cut off can be calculated after first obtaining both of the high frequency poles

$$\omega_{HP1} = \frac{1}{\left(\frac{c_\pi}{2} + \frac{c_u}{2}(1-k)\right)2r_\pi||R_S}$$

$$\omega_{HP2} = \frac{1}{\frac{c_u}{2}\left(1-\frac{1}{k}\right)R_L||2R_C}$$

Where k is the miller gain which is given by

$$k = -g_m R_C \frac{R_L}{R_L + 2R_C}$$

$$k = -320\frac{V}{V}$$

So, the pole locations are

$$\omega_{HP1} = 31.01 Mrad/s$$

$$\omega_{HP2} = 31.2 Mrad/s$$

And the associated time constants are

$$\tau_{Hp1} = 32.2ns$$

$$\tau_{Hp1} = 32.05ns$$

Because these are so close in value, I cannot approximate by just using the dominant pole

$$\tau_{H3dB} = \sqrt{\tau_{Hp1}^2 + \tau_{Hp2}^2}$$

τ_{H3dB} =45.43ns

ω_{H3dB} =22.01Mrad/s

$$f_{H3dB} = 3.5MHz$$

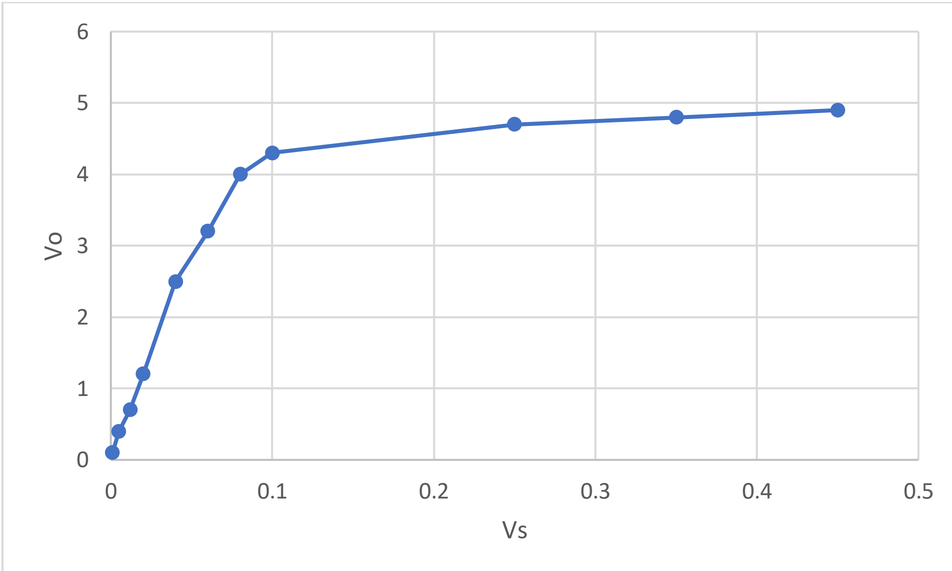
Comparison of measured and calculated values:

	Measured	Calculated
$\boldsymbol{A_d}$	$-168\ V/V$	$-159.2\ V/V$
$\boldsymbol{f_{H3dB}}$	$7.26MHz$	$3.5MHz$

Discussion[Calculated vs Measured Values]:

- The measured and calculated results match up quite nicely which is reassuring that the methods and tools taught in class are sufficiently accurate in their delivery to make the results meaningful. As is always the case, there is more error in the high frequency analysis than is usual present in the low frequency analysis or gain calculation. This is due to necessary approximations being made such as miller’s theorem and other such approximations to decouple the output stage from the input stage and deal with the high frequency capacitors

C.

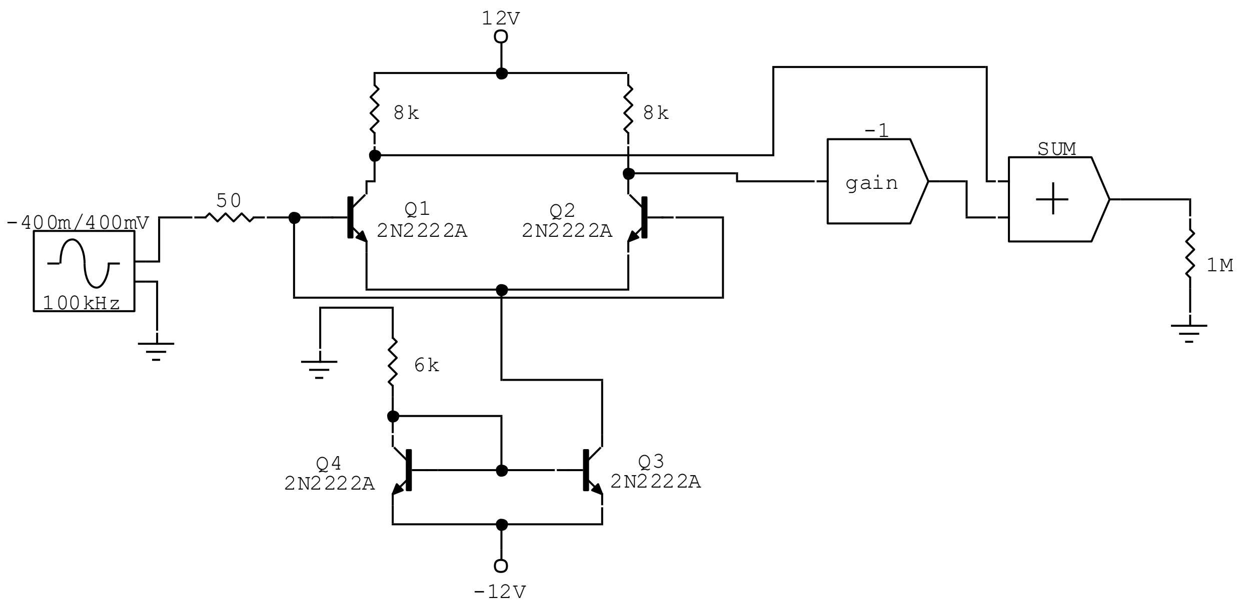


Discussion[Vo/Vs Plot]:

- At this mid band frequency, it is clear where the non linearity begins with this amplifier. As the input signal is steadily increased, the gain remains linear up until a point and then it levels off to become a steady value. This is due to limitations with the transistors and occurs when the active region has been left and the transistors are entering saturation

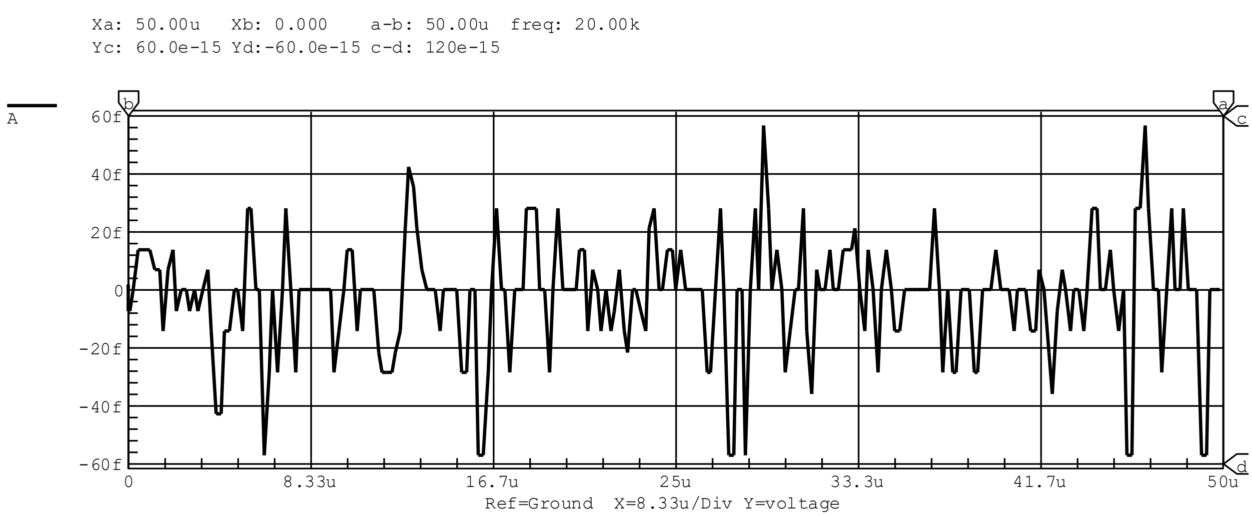
D.

A common signal is applied to both transistors



Common Mode Circuit with 0.4Vp input

Because this is a differential amplifier, when a common signal is applied the desired output is 0V



Transient Response

It can be seen from the oscilloscope that the output for a common mode signal is indeed very small (on the order of femtoVolts ie: 10^-15V), however due to non idealities there is still some signal being amplified

To find the common mode gain

$$A_{cm} = \frac{V_o}{V_{icm}}$$

$$A_{cm} = \frac{30fV}{400mV}$$

$$A_{cm} = 0.075p\frac{V}{V}$$

The common mode gain is extremely small as expected (0.075 picoVolts/Volt)

To find the common mode rejection ratio

$$CMMR = \frac{|A_d|}{|A_{cm}|}$$

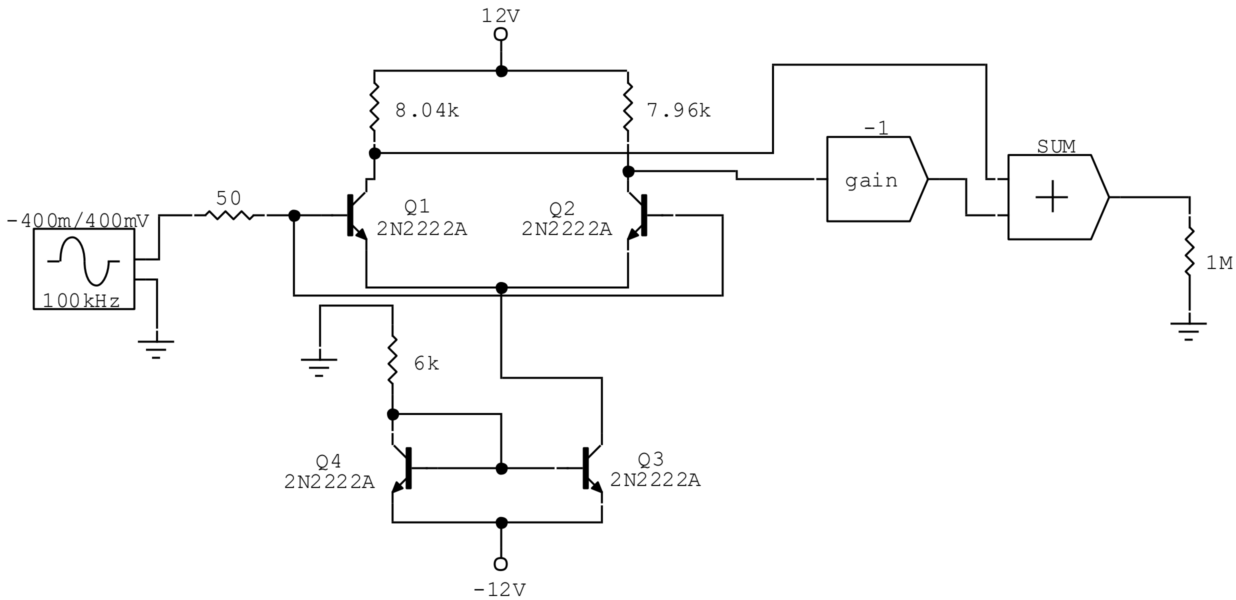
$$CMMR = \frac{|-168|}{|0.075p|}$$

$$CMMR = 2.24P\frac{V}{V}$$

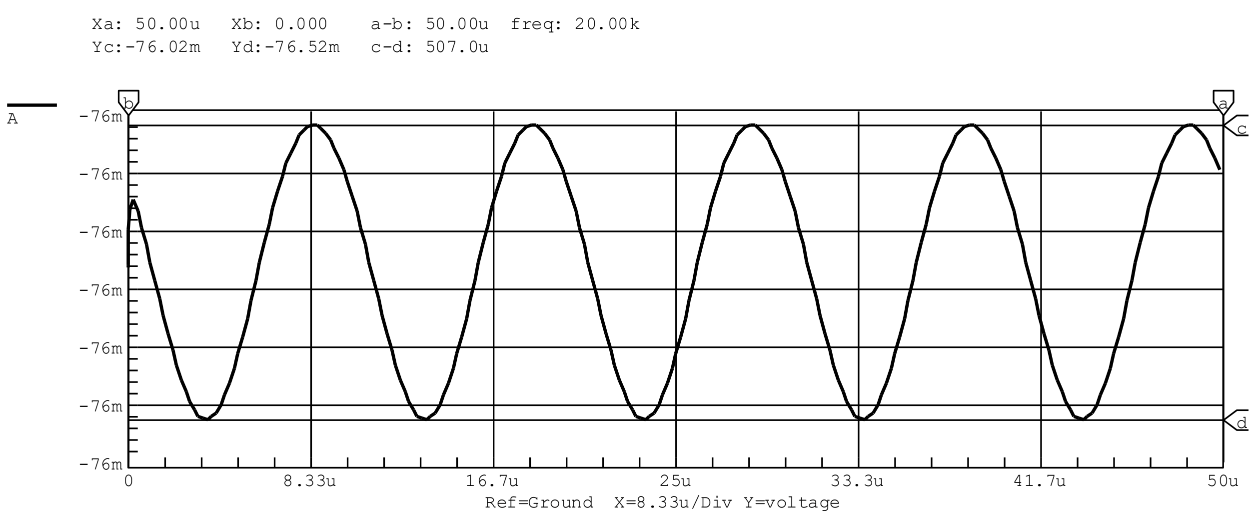
$$= 307dB$$

And the common mode rejection ratio is extremely large as expected (307 Decibels)

Increasing/Decreasing collector resistors by ½%:



Common Mode Circuit with modified resistors



Transient Response

It can immediately be seen that changing each resistor by only half of a % is causing the differential amplifier to now amplify this common mode signal

To find the common mode gain

$$A_{cm} = \frac{V_o}{V_{icm}}$$

$$A_{cm} = \frac{253.5uV}{400mV}$$

$$A_{cm} = 633.75u\frac{V}{V}$$

The common mode gain is now 633.75 microVolts/Volt

To find the common mode rejection ratio

$$CMMR = \frac{|A_d|}{|A_{cm}|}$$

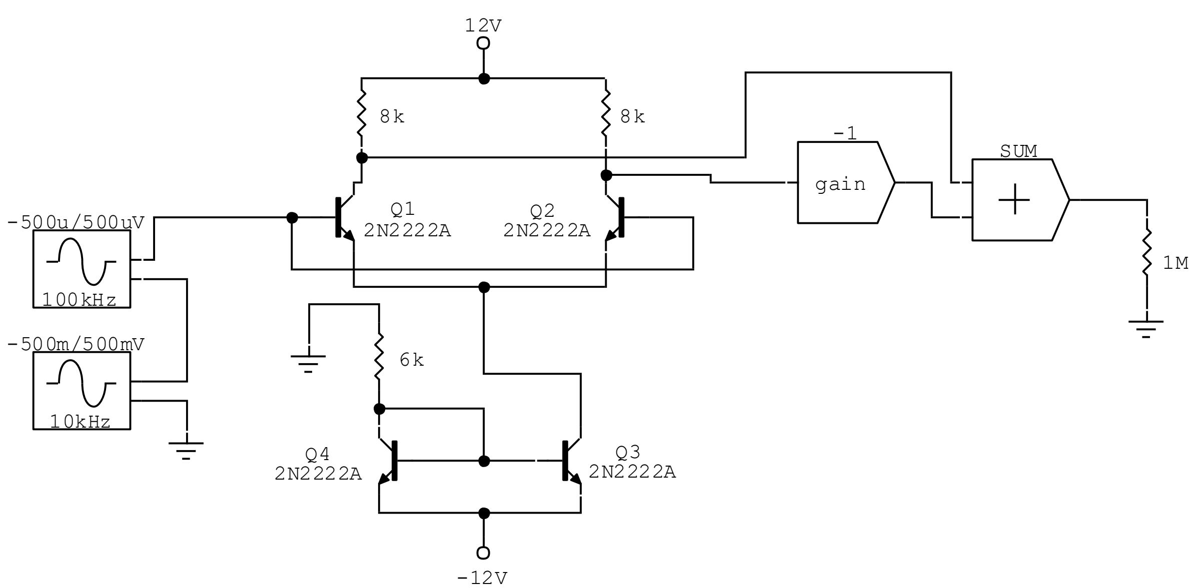
$$CMMR = \frac{|-168|}{|633.75|}$$

$$CMMR = 265.1k\frac{V}{V}$$

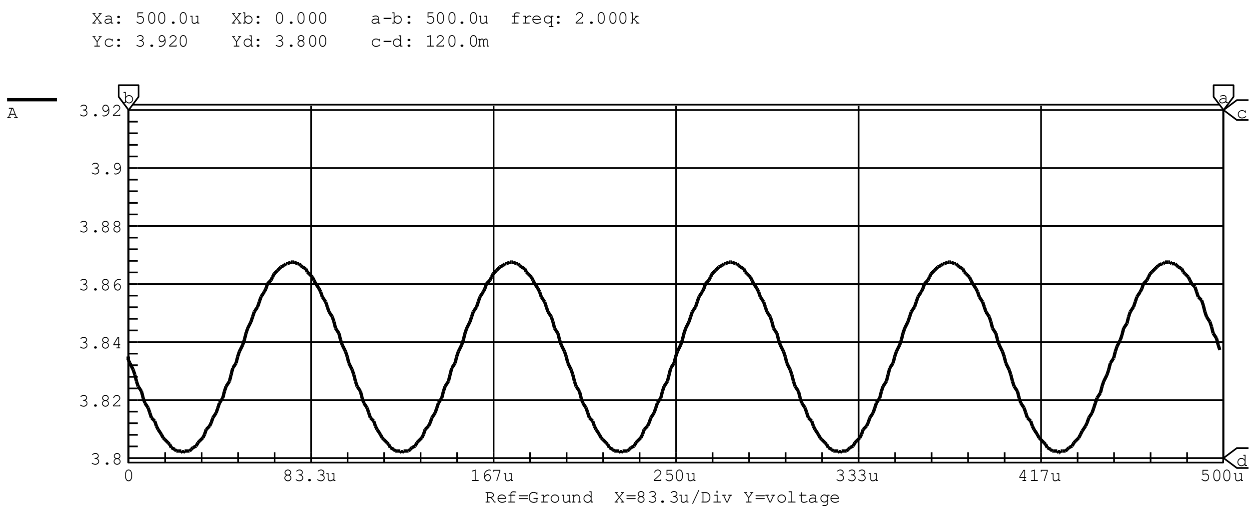
$$= 108.5dB$$

And the common mode rejection ratio is now much smaller (108.5 Decibels)

E.



Differential Signal and Common Mode Signal Circuit



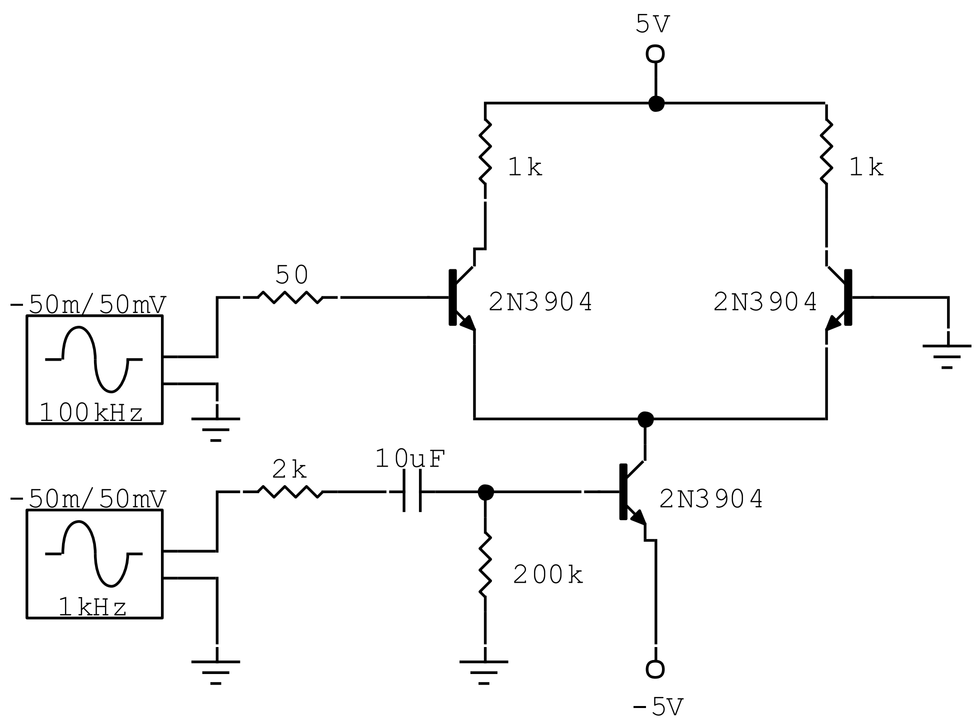
Differential Output Response

Summary[Part III]:

- In this section, the differential amplifier was examined. This amplifier is composed of more pieces than were seen in the beginning of the course when only common type amplifiers were being looked at. As the name suggests, this amplifier seeks to amplify the difference between signals as there are two points where input signals can be delivered. In doing this it is designed to reject common signals in the form of the common mode rejection ratio. Due to non-idealities with the transistors, this is not perfectly achieved. It was seen that even when two identical signals were delivered, some small portion is still amplified at the output. However, this effect is very small and the amplifier worked quite well at reducing this common mode gain to be as small as possible. When the resistor values were altered such that there was a 1% difference between them, this effect was compounded and more of the common mode signal was present at the output.

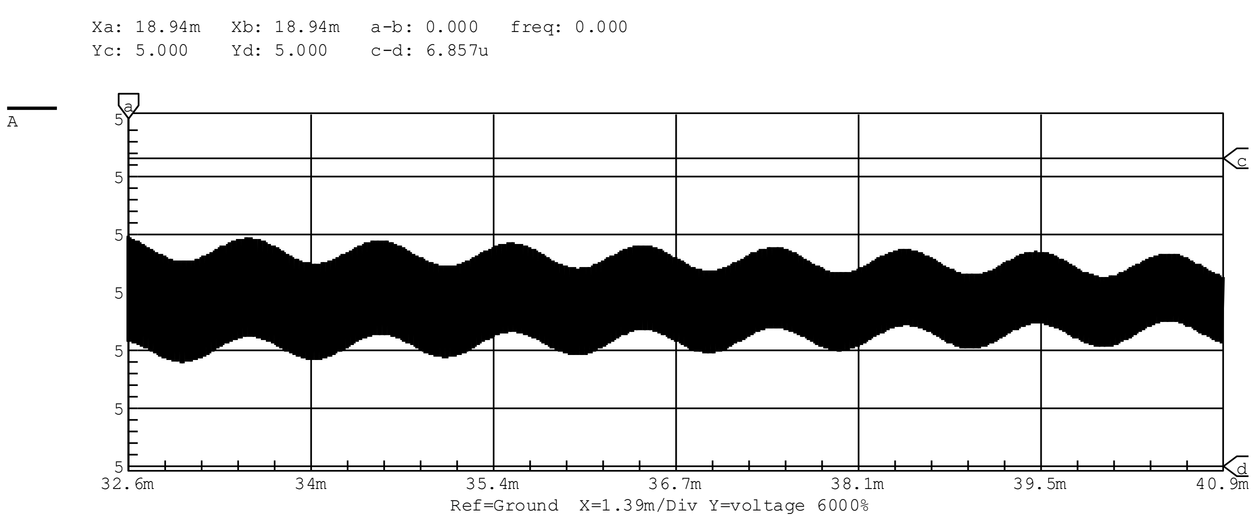
Part IV

A.



AM Modulator Circuit

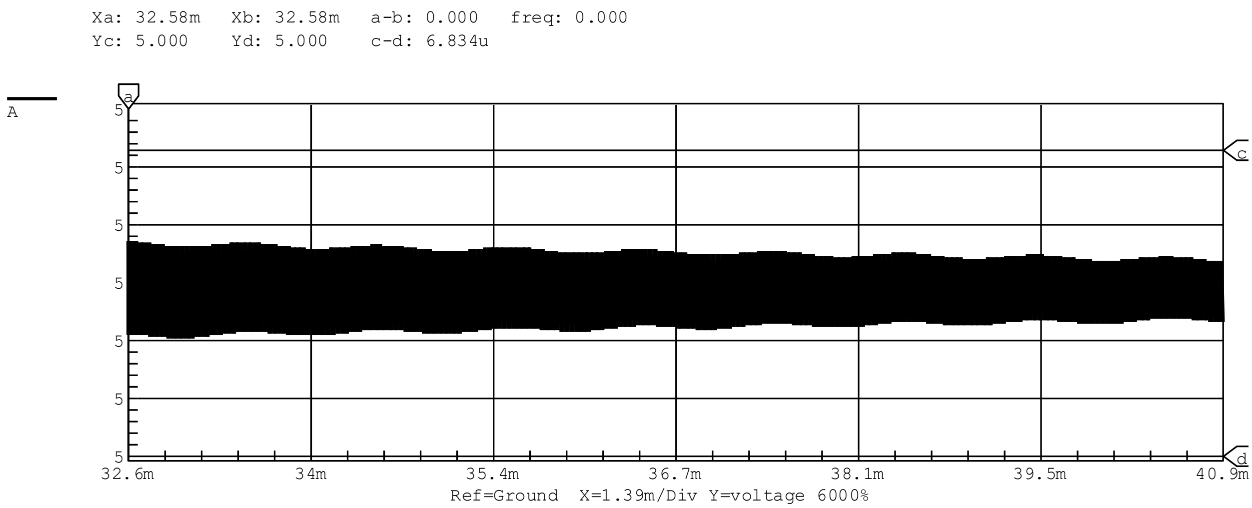
I apply a 50mVp, 1kHz sine wave to the input of the modulator. This is the differential output



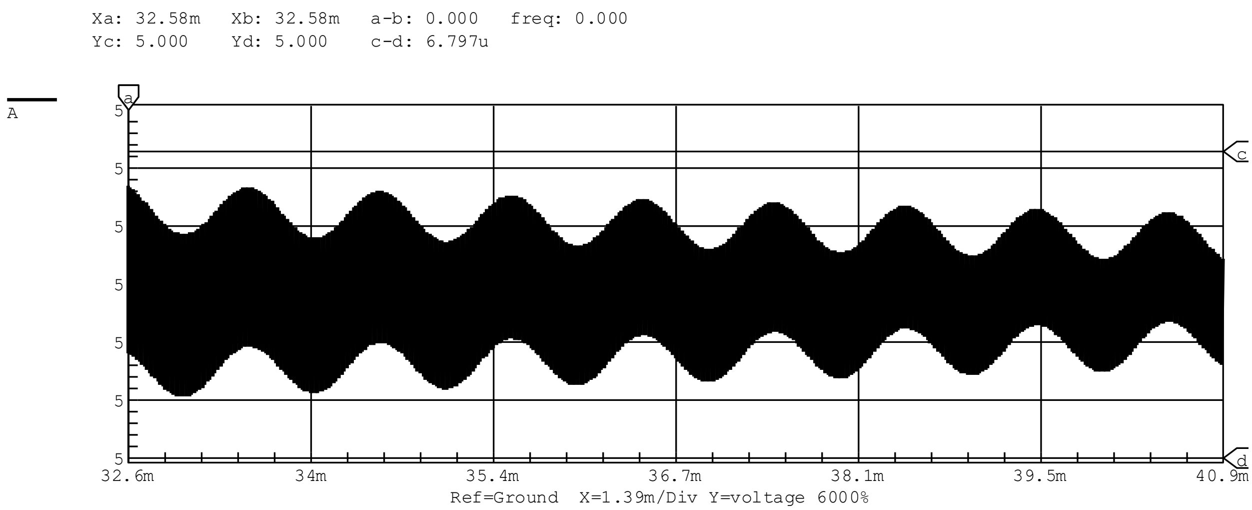
Transient Analysis for 50mVp input

B.

To see the effect of different input voltages on the AM Modulator, I can change the input signal to be 10mVp and 100mVp



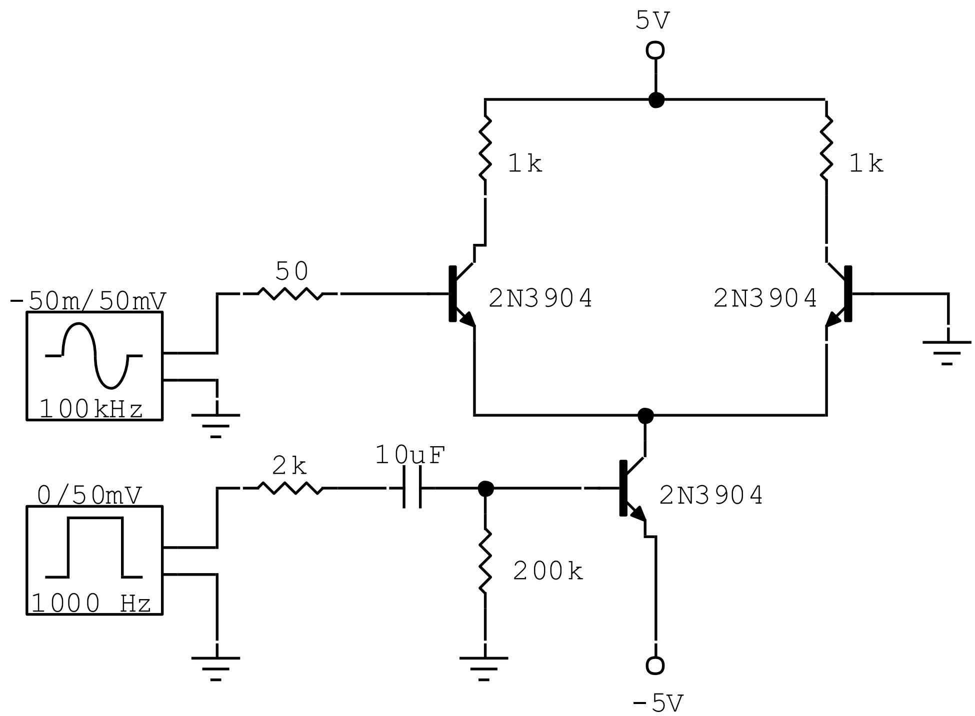
Transient Analysis for 10mVp input



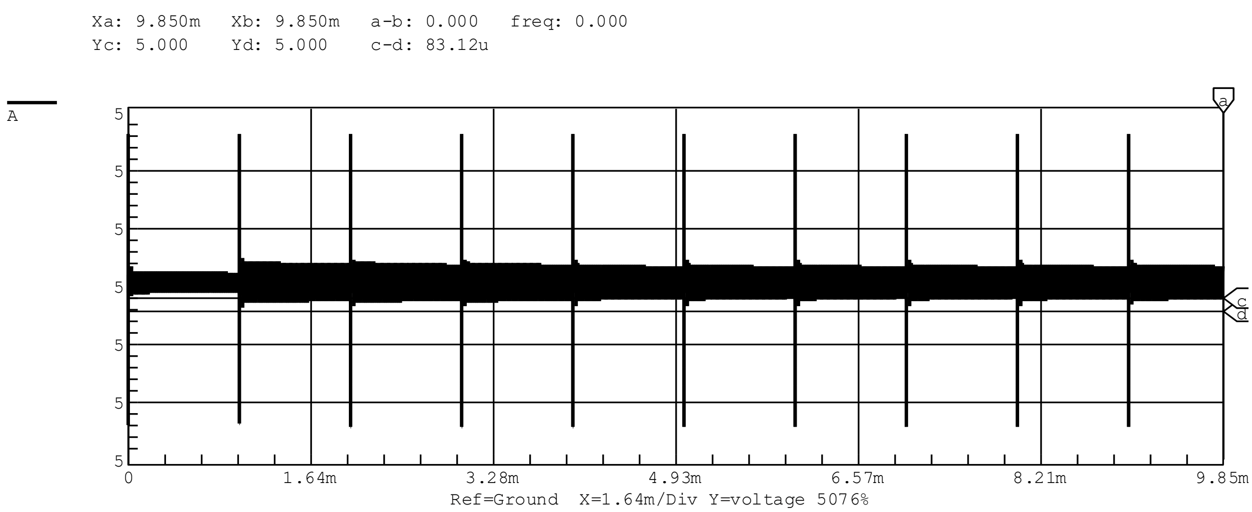
Transient Analysis for 100mVp input

It can be seen clearly from these differential responses that higher input amplitudes result in more distortion. I experimented with various input voltages and found that the largest input signal that did not result in a distorted output signal was approximately 80mVp

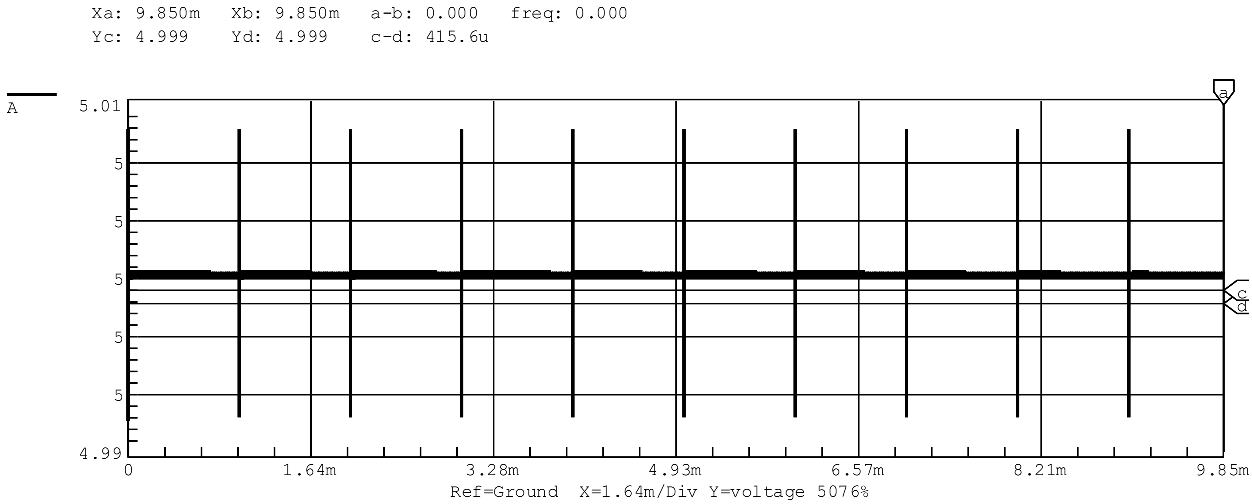
C.



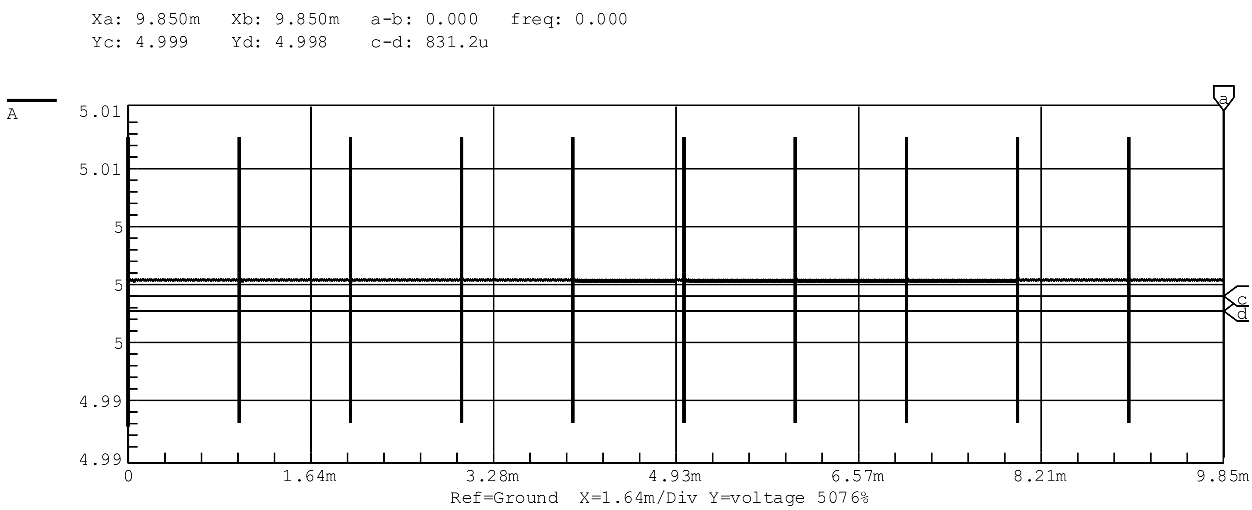
AM Modulator Circuit with Square Wave input



Transient Analysis for 50mVp square wave input



Transient Analysis for 10mVp square wave input



Transient Analysis for 100mVp square wave input

The result for the output signal is the same in the case of the square wave input

Summary[Part IV]:

- In this section, the AM Modulator was examined. The modulator works by using a carrier signal to deliver an input signal. This process of imposing an input signal onto the carrier signal is known as modulation. Combining these signals changes the nature of the carrier wave and encodes the necessary information from the input signal inside it. This technique was examined by applying a sine wave and a square wave signal as an input and steadily increasing the peak voltage to examine the results. In both cases the result was the same. Increasing the peak voltage past a certain point resulted in the original input signal becoming distorted and information being lost. This demonstrates why the process of modulation is useful to a point, but there are limitations when the input signal starts becoming large relative to the carrier signal.